Design of Single Electron (SEEL) Encoded Logic Based Hamming Code IC

Dr. J. Gope (MIEEE, CE), S. Chakraborty, I. Misra, R. Mandal, T. Chatterjee

Dept. of ECE, Camellia School of Engineering & Technology, MAKAUT, India

ABSTRACT: *Digital information system do poses errors, these errors are the consequence of path delay in communication system as some sort of errored signal processing to achieve an error free information. Error detection circuits are pivoted several tropology's are being implied since the last three decade. In the past CMOS era we see how single electron transistor are incorporated to achieve error free signal. The authors in this article uses Single Electron encoded logic (SEEL) to detect possible error using hamming code and use the same process to multiply the error with maximum speed. The resultant circuit is unique of its kind as SEEL Based Hamming Code is yet to be used profoundly.*

Keywords- *CMOS, Digital information, Errors, Hamming Code, Path Delay, SEEL.*

I. INTRODUCTION

Recent research endeavor in SET offers novel notions and aims to revolutionize the random access memory and digital data storage technologies by the dawn of the next decade. The basic physics and applications of nano electronic device based 'Single electron transistor [SET]' reveals that it is intrinsically capable of controlling the transport of only one electron. This has attributed SET as a key element of current nm ranged VLSI/ULSI research of nanotechnology and subsequently offers low power consumption and high operating speed. It is a next generation switching device and employs controlled electron tunneling to amplify the current. SET have engrossed Researchers worldwide for achieving high functional density, low power consumption, extremely fast switching, high integration density, simplicity and robustness. The maneuvering of Single Electron Device is centered on the Coulomb Blockade principle. It was principally demonstrated in a nanostructure and was observed and studied at a very low supply voltage by Gorter [1]. The main constituent of the SET circuits is the Tunnel Junction amidst which single electrons can transport in a controlled modus [3]. Thus the candidature of SET to replace CMOS elucidates incredible potential for the advancement of future miniature circuits. Hitherto, workings on gate based novel half-adder [2], set logic gate families [4], single-electron full-adder [5], digital-quantizers [6], NAND gate [7], Programmable Logic Arrays [8] have been reported in scientific journals of repute. SEEL was derived from SET. The modus operandi of SET based SEEL technology is the tunneling of the electron in a controlled manner, using this technology several new devices are being designed now a days. SEEL technology from its very inception catered research interest owing to its high functional density low power consumption. It is because of its switching speed that is nearly equal to the electron speed SEEL popularized manifold [9]. The potential of SEEL technology lies on its simplistic structure derived from SET. The present attempt is to improvise SEEL based IC designing for communication engineering, this IC is to be integrated in Error Correctional Hardware.

II. SET BASED LOGICAL INTERRELATIONS

The scaling down of transistors beyond 10nm gate length was predicted in ITRS 2013 [10]. This has brought into Ultra-Thin. Body (UTB) transistors having excellent device features. SET is quite similar to ordinary MOSFET but the only distinction is that it has a tunnel junction. A Coulomb Blockade is observed in this type of configuration until & unless the Coulomb Energy is greater than the static energy the Coulomb Blocked can of be capitulated. The simplistic, robust, and straight forward device configuration is exhibited in a single electron box. The tunnel junction includes a metal in one side of the surface. Due to the size and capacitance C of the tunnelling of only one so that it can generate a noticeable change e/c of voltage across the junction. A single electron can pile up one bit of information so the power consumption will be reduced [11, 12]. Thus SET based single electron devices manipulate individual electron and finally utilize them in the form of the electron devices. Empirical results showed how the momentum power product of SET is fare-casted to lie close the quantum limit which is set by the Heisenberg's Uncertainty principal. The processing speed of this type of devices is likely to be similar to the electronic speed. Similarly, delicate sensitivity is about five orders of degree heightened than conventional solid-state CMOS transistors. This is the basic theorem about SET. Now using the SET we are designing various kinds of logical parts.
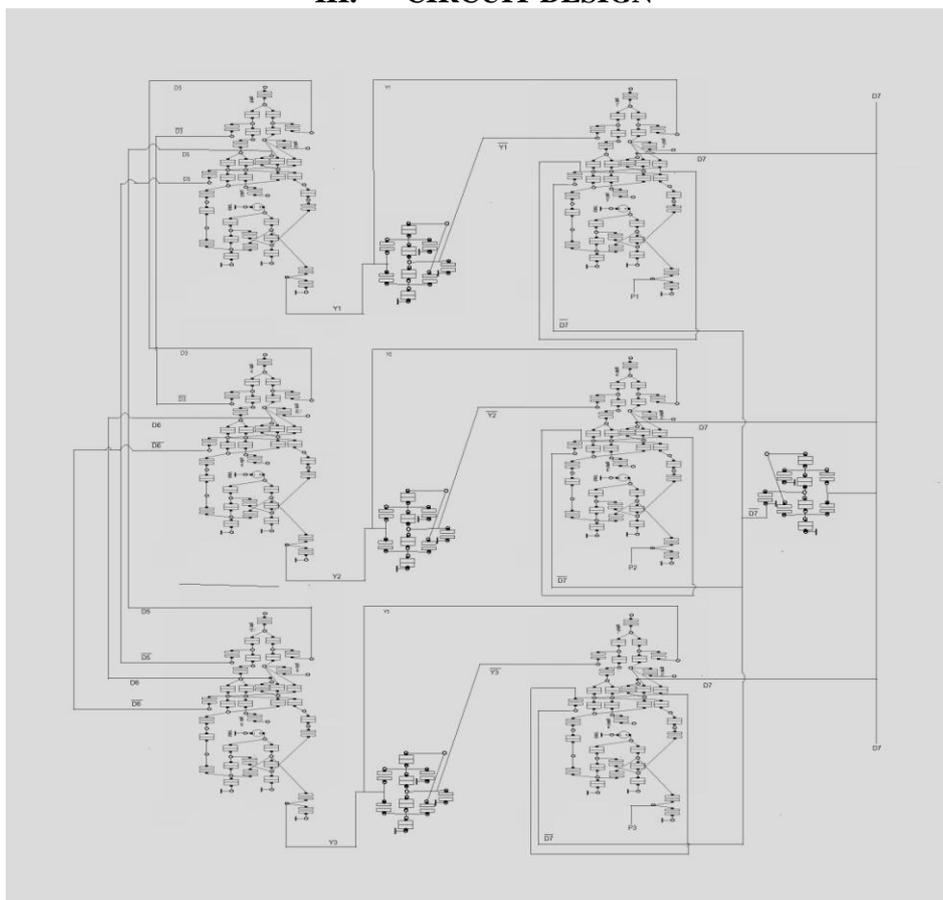
III. CIRCUIT DESIGN

Fig. 1: SET based Hamming Code Circuit

This is the SET based circuit diagram of Hamming code. Here every XOR gate represented by its equivalent SET circuit. Each gate is made of 20 tunnel junctions and 15 capacitors. For the 1st XOR gate D$_3$ & D$_5$ are the inputs and we also used the inverted form of these inputs. Y$_1$ is the output of the 1st XOR gate. Y$_1$ & D$_7$ are the inputs of the 2nd XOR gate. Hare also we used the inverted form of the inputs.

Similarly D$_3$, D$_5$ and D$_5$, D$_6$ are the inputs of 3rd & 5th XOR gate respectively Y$_2$ & Y$_3$ are the outputs of these two gates respectively. Y$_2$&D$_7$ are the inputs of 4th XOR gate, form which we get the output P$_2$ and Y$_3$ & D$_7$ are the inputs of 6th XOR gate from which we get the output P$_3$. Here also in every XOR gate the inverted form of each inputs were used for our convenience.

Due to the logical synthesis of the proposed circuit the wirings or interconnects are put a little bit apart form each other. Regarding this, the wirings are became longer but during fabrication it is obvious that such wirings will be limited considerably. This will intern reduced the propagation delay as well as increase the operating speed.

IV. CONCLUSION

Research in error correcting hardware in communication engineering attained considerable heights since the dusk of last century. CMOS made Hamming Code circuit are available today but they suffer from the intrinsic drawbacks of CMOS. Thus here the authors attempted to improvise the Hamming Code circuit using SEEL technology, and thus a SEEL based modelling is reported here. The attributes of SEEL based designing is that it offered greater flexibility in nano regime designing and subsequently the speed – power consumption factor satisfactorily dominated CMOS technology. Moreover, the simplicity and robustness of SEEL circuit was quite apparent in the designed circuit. This is why the authors do advocate for SEEL technology rather age old CMOS technology in rendering next generation communication ICs.

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